ABSTRACT OF THE DISCLOSURE

A semiconductor memory capable of attaining a low voltage, a high-speed operation, low power consumption and a high degree of integration is obtained. This semiconductor memory comprises a floating gate electrode, a first source/drain region having a diode structure employed for controlling the potential of the floating gate electrode and a second source/drain region formed to hold a channel region between the same and the first source/drain region. Thus, when a channel of a transistor is turned on in reading, a large amount of current flows from the first source/drain region having a diode structure to a substrate, whereby high-speed reading can be implemented. Further, a negative voltage is readily applied to the first source/drain region having a diode structure, whereby a low voltage and low power consumption are attained and the scale of a step-up circuit is reduced, and hence a high degree of integration can be attained.